easics
get our logic in your system

30 YEARS IN BUSINESS
founded 1991

product sheet
nearbAI

nearbAI™

IP cores for ultra-low power AI-enabled chips

each nearbAI core is an ultra-low power neural processing unit (NPU) and comes with an optimizer / neural network compiler. it provides immediate visual and spatial feedback based on sensory inputs, which is a necessity for live augmentation of the human senses.

- optimized neural network inferencing for visual, spatial and other applications
- unparalleled flexibility: customized & optimized for the customer's use case
- produces the most optimal NPU IP core for the customer's use case: power, area, latency and memories trade-off
- minimized development & integration time

ideal for battery-powered mobile, XR and IoT devices


3D / SPATIAL DETECTION


FACE DETECTION


FACE ID


FACE BLURRING

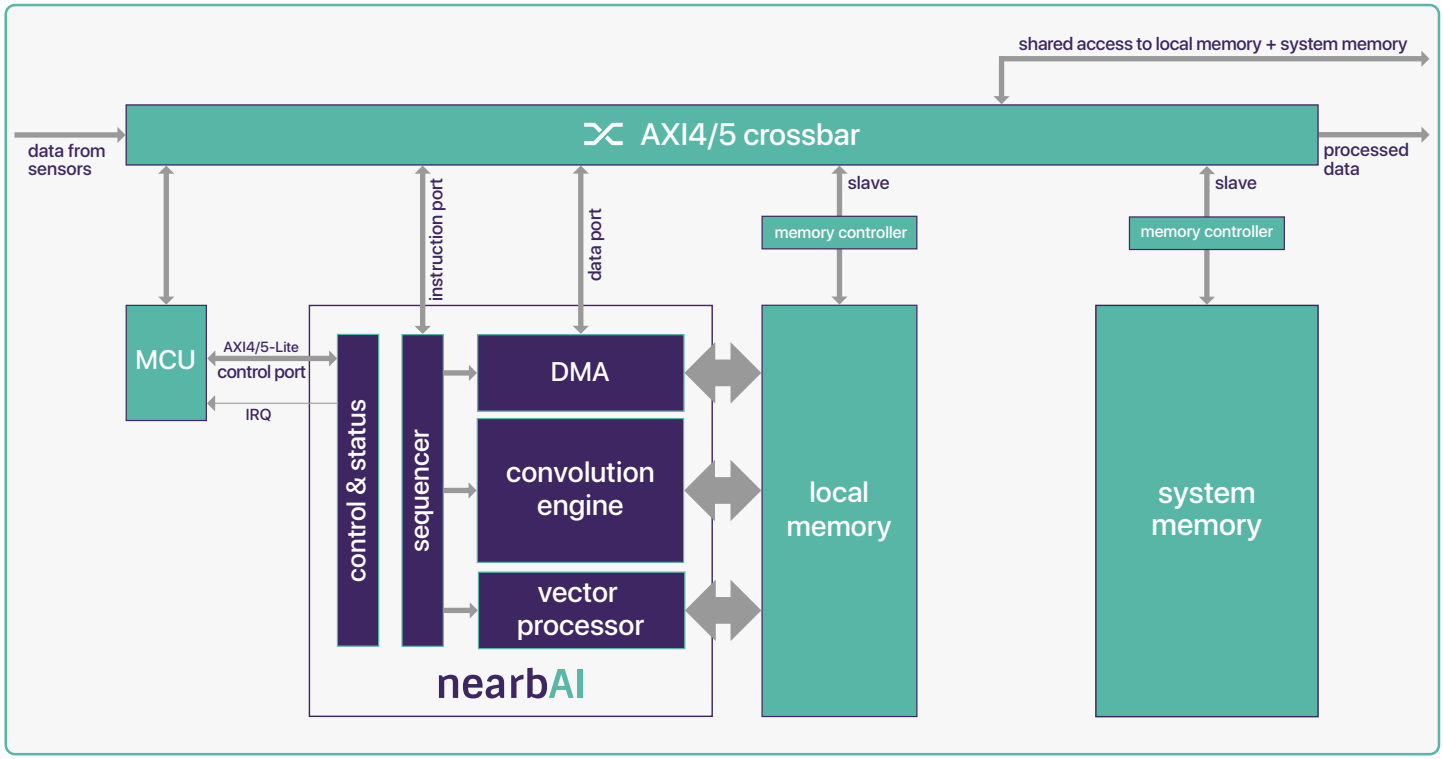

IRIS ID


GESTURE RECOGNITION /HAND TRACKING


OBJECT DETECTION


OBJECT RECONSTRUCTION

TEXT DETECTION



why nearbAI?

highly computationally efficient and flexible NPUs

enable lightweight devices with long battery life ... with ultra-low power, run heavily optimized AI-based functions locally

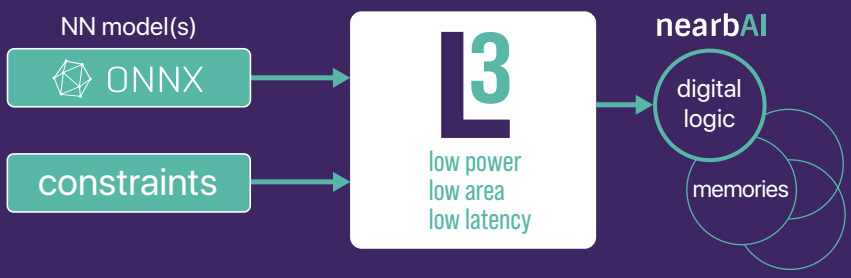
enable truly immersive experiences ... achieve sensors-to-displays latency within the response time of the human senses

enable smart and flexible capabilities ... fill the gap between "swiss-army knife" XR / AI mobile processor chips and limited-capability edge IoT / AI chips

nearbAI™

IP cores **for ultra-low power AI-enabled chips**

L3 - optimizer platform for ASIC



optimized for customer-specific use case

specifications

• L3 optimizer for optimal power, area and latency balance	• power: supports sub 1 mW always-on visual / spatial applications
• NN compiler for firmware updates in the field	• configurable number of parallel MACs in convolution engine: 16 to 8192
• zero-latency NN switching - e.g., face ID NN gets faces only from face detection NN, multiplexed with other NNs	• integrates seamlessly with a wide range of RISC-V and ARM processor cores
• top computational efficiency for crystallized AI functions, yet programmable and field-upgradable	• typ. 4nm for mobile XR processor chip • typ. 22nm for compact extreme edge AI chip
• configurable MAC accuracy: independent coefficient and data quantization, 4 to 16-bit, single-bit granularity	• supports model zoo of CNN / RNN / LSTM, and tailored customization
• long-term support: 5+ years	*for additional information, please contact your local sales representative*

process

1. NN model(s) & constraints
2. profiling, L3 optimization & compilation
3. custom benchmarking report
4. ASIC customization, integration & verification
5. ASIC tape-out

delivery options **incl. customization**

- standard off-the-shelf IP core(s)
- customized IP core(s)
- IP core(s) + ASIC integration services
- IP core(s) + full ASIC design services

ISO 9001 2015 CERTIFIED

let's do a custom benchmark together:

provide us with your use case:

- **quantized or unquantized NN model(s):** ONNX, TensorFlow (Lite), PyTorch, or Keras
- **constraints:** average power & energy per inference, silicon area, latency, memories, frame rate, image resolution, foundry + technology node

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V1.3