nearbAI™

The Smart & Flexible
IP Cores for XR Devices

easics has +30 years experience in custom DSP and image sensor chip design and is now offering nearbAI, a family of digital IP cores. nearbAI is developed from the ground up and optimized for ASICs / ASSPs / SoCs to be used in XR devices.

Each nearbAI core is an ultra-low power neural network inference engine and comes with an optimizing neural network compiler. It provides immediate visual, aural and other feedback based on sensory inputs, which is a necessity for live augmentation of the human senses.

nearbAI powers functions such as scene segmentation and reconstruction, object and face detection and recognition, foundational to consumer and enterprise XR applications.

2ms
INFERENCE TIME

easics
get our logic in your system
www.easics.com

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ANSWERS TO YOUR NEEDS

Ultra-fast Response Time

- Live feedback within response time of human senses, from sensors to in-glass displays
- Real-time pattern recognition with fixed inference latency; face detection in 2 milliseconds

Zero-latency Switching

- Continuous multiplexing between multiple neural networks, on the same nearbAI core
- One neural network detects regions-of-interest and passes them to the next network, on the same nearbAI core
  Example: feed detected faces into face recognition network

Low Power

- Maximized battery performance
- Low heat dissipation
- Reliable (less likely to run out of power whilst in use)
- Environment friendly

Scalable & Flexible

- Optimized power-performance-area (PPA), based upon customer needs
- Silicon technology agnostic: 40nm down to 5nm and beyond
- Programmable using the optimizing compiler during the product lifecycle

Optimizing nearbAI Compiler

- Reads in your neural network in ONNX format using TensorFlow, Keras, PyTorch, mxnet
- Includes profiler with full layer-per-layer visibility
- Record-breaking utilization up to 95%
- Single-bit granularity data types

Secure OTA Updates

- Field upgrades of neural network models and weights using secure SW Over-the-air updates
- Lifecycle management
- Supports offload engine/processor outside IP core

Local processing

- Each nearbAI IP core operates standalone:
  - Ultra-low latency
  - Privacy conserving: local removal of sensitive data
  - High level of data security and reliability
- nearbAI in datapath between sensors and XR processor
- Sensor fusion
- Supporting image sensors, ToF, LiDAR, microphones etc.
- Cloud interoperability (optional) with low system latency

Unique Small Footprint / Low Cost

- Smallest silicon area
- Lowest PCB cost
- No additional XR accelerator chips needed

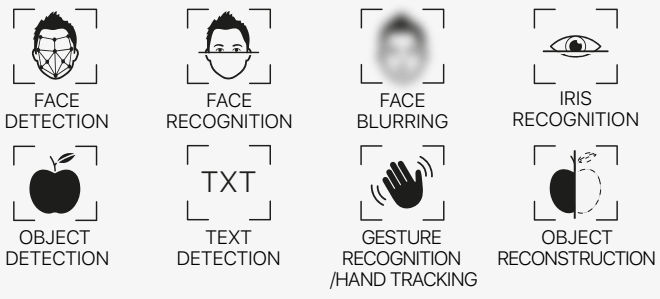
Easy SoC Integration

- Application & integration templates available
- Supports Linux API & bare metal
- Peripheral and sensor interface blocks supported
- Support & integration team with +30 years experience / first-time right

Time-to-market Acceleration

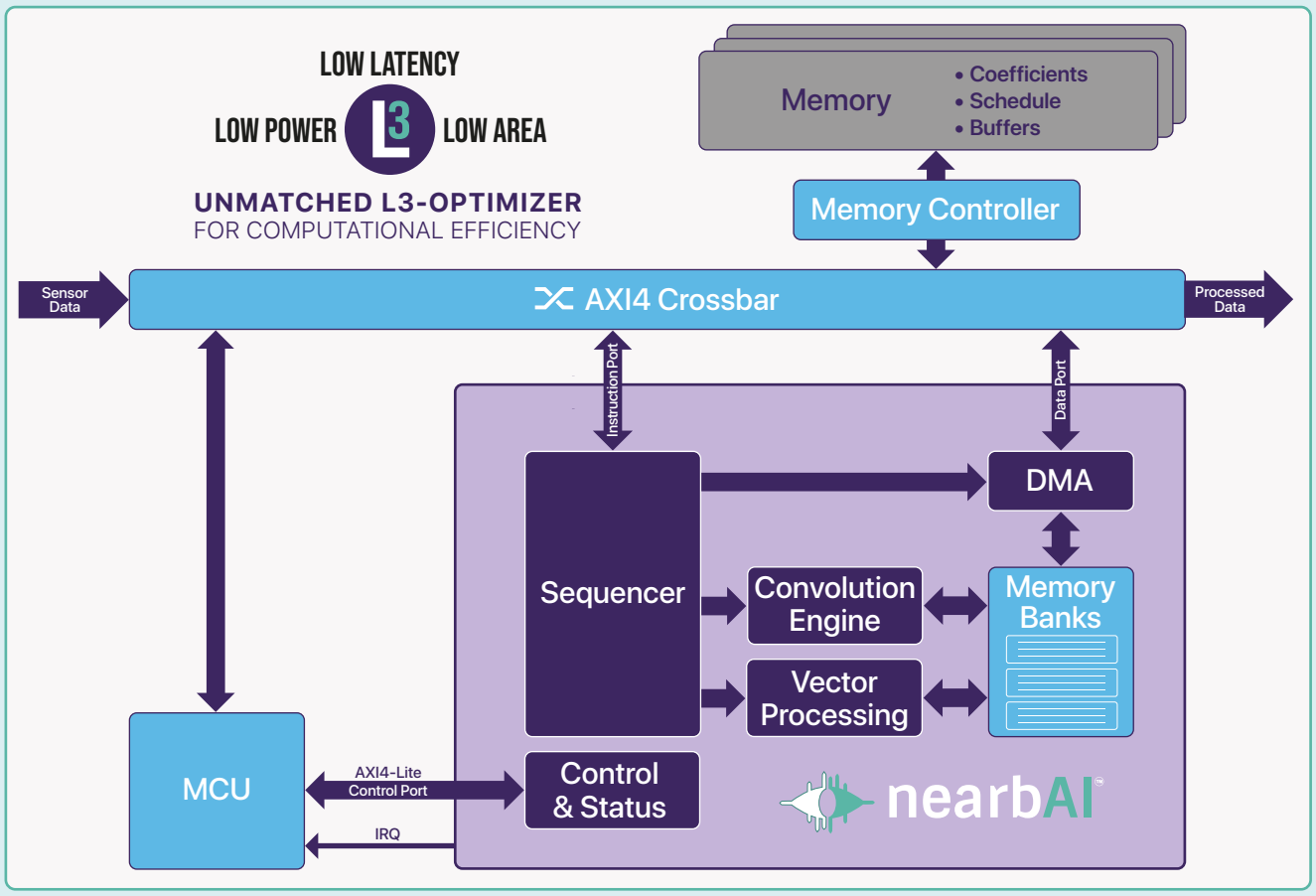
- Very fast FPGA prototyping in path towards ASIC/ASSP
- Smooth integration of the easics IP core
- Efficient deployment and field upgrades via OTA

Function Examples

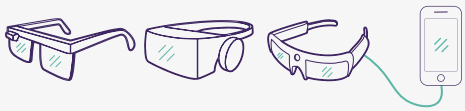


First-time right

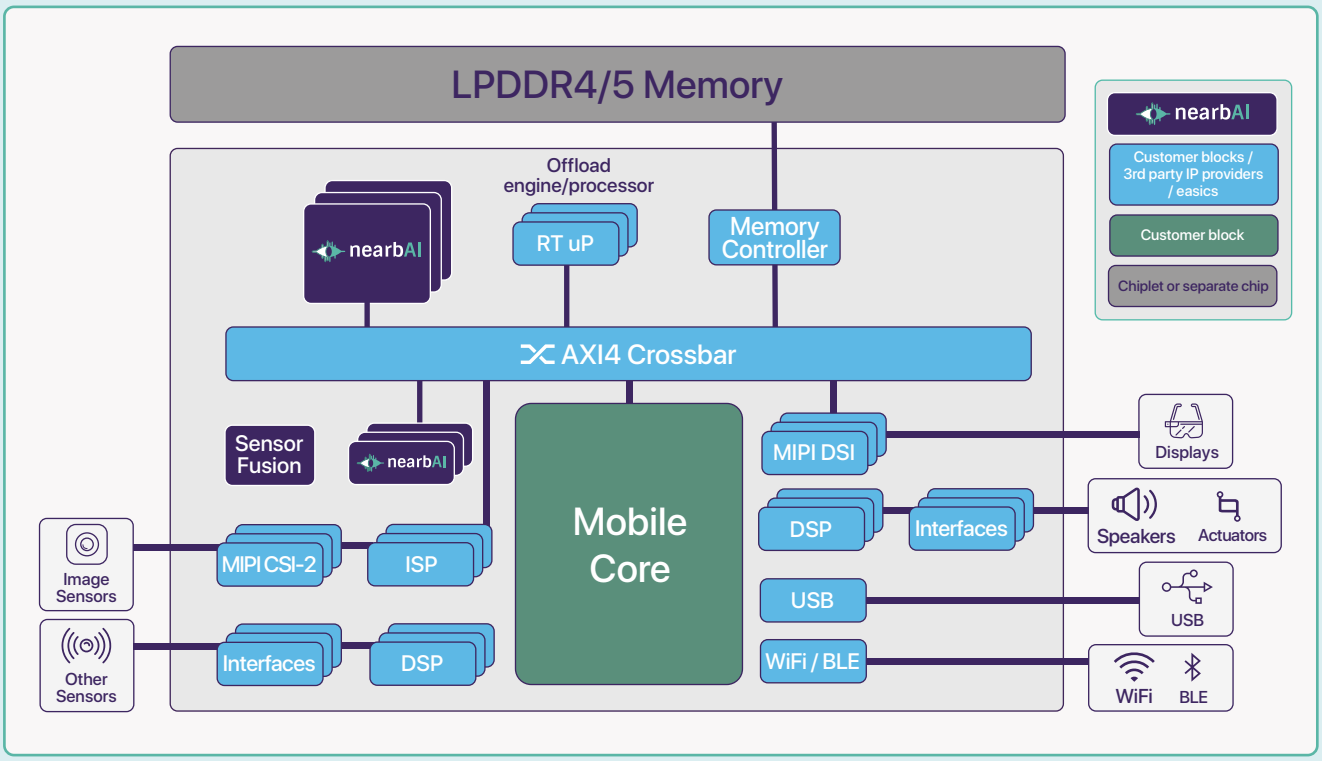
IP CORE & PERIPHERALS



nearbAI™ *Ideal for both standalone and tethered XR devices*



MOBILE XR PROCESSOR CHIP INTEGRATION



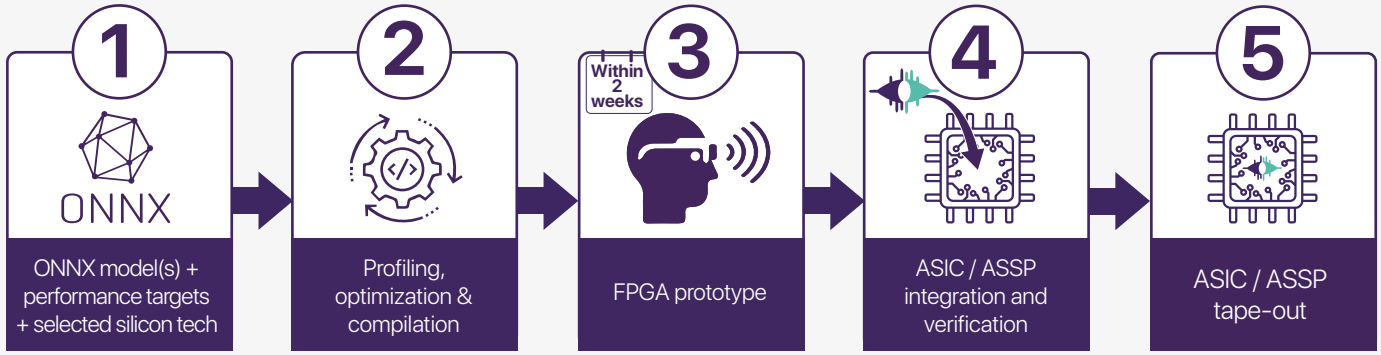
Specifications - nearbAI IP cores for XR devices optimized for ASICs / ASSPs / SoCs

• Top computational efficiency for crystallized AI functions, yet programmable and field-upgradable	• Power: As low as sub 10 mW, depending on application and silicon technology
• Typ. 5nm for mobile XR processor chip • Typ. 22nm for compact extreme edge AI chip	• Compatible memories (multi-vendor): LPDDR4/5 DRAM, SRAM and ROM
• Configurable number of parallel MACs in convolution engine (16 to 4096)	• Integrates seamlessly with major microprocessor cores
• Configurable MAC accuracy: independent coefficient and data quantization, 4 to 16-bit, ***single bit granularity***	• Wide range of CNN / RNN / LSTM supported
• Configurable internal memory bank sizes and bus widths	• Supports product life cycles of 5+ years

nearbAI IP cores are ideal for both standalone and tethered XR devices (AR / VR / MR glasses and headsets)

For additional information, please contact your local sales representative or visit our website www.easics.com

Efficient Delivery



Delivery Options

- Standard off-the-shelf IP core(s)
- Customized IP core(s)
- IP core(s) + ASIC integration services
- IP core(s) + full ASIC design service

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easics is a market leader in semiconductor IP licensing & digital chip design. We provide unique competence and development platforms that lead to first-time right, reliable and optimized logic and software that is maintainable by the customer. Our main target market is to support leading OEMs and semiconductor companies with custom designs and customizable IP blocks for these smart embedded processing systems that can be realized in ASICs / ASSPs / SoCs and in FPGAs.

ISO 9001 2018 CERTIFIED

+30 YEARS IN BUSINESS

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