



Always looking for colleagues to ride the digital wave

You're interested in standing on the front line of digital evolution and want to be part of the newest improvements in the technological world?

Great!

You want to be part of the practical applications of digital designs, from idea to finished product?

Perfect!

You have a Master of Science or PhD degree in Electronics Engineering, Computer Science/Engineering, Applied Mathematics, or similar?

Terrific! Read on!

We make the world a smarter place

Easics is the reference in smart electronic systems design. Our customers are world-leaders in their field. They give us interesting and rewarding challenges for first-of-a-kind applications. Take for example: neural net inference at the extreme edge, a radiation-hardened camera for earth observation satellites, top-notch hearing implants helping newborns and grandmas alike, power-harvesting wireless tags, ...

We discuss the complex algorithms and requirements with our customers and turn them into cutting-edge reality, solving the challenges inherent to silicon implementations. We model these challenges in software and optimize all layers of abstraction. Trade-offs in performance, power consumption and area are made along the way, resulting in the physical realization: an FPGA, a System-on-Chip or a custom-tailored ASIC at the heart of our customer's products.

We'll make you an expert, no worries

Whether you are an eager starter having just obtained your Master's degree or a seasoned professional, we'll guide you through our design methodology and introduce you to our vast body of expertise. Easics is known to be a 'learning' company, one that will give you the chance and time to become an expert, no matter what your previous experience is. You will join the easics academy from day one.

You will work on projects in diverse domains, making high-level models, mastering the intricacies of timing and parallelism, running tests in our lab or discussing requirements and architecture with the customer. Our people work in teams with high autonomy, and they are always ready to help each other out.

We can't wait to see you join our growing team

Design and Verification Engineer Full time

We are currently seeking a highly motivated individual as a Design Engineer. You'll be working on challenging new projects including FPGA and digital ASIC design and verification, embedded software design, modeling and verification of large digital systems, Python, C++, SystemC, VHDL, (System)Verilog, GNU/Linux. You will be tasked with understanding, implementing and verifying your first modules. As time passes, you take on a larger variety of tasks and responsibilities.



Design Engineer

(FPGA, ASIC, embedded software)

Whether this is your first application, or you've already had a first job experience, we'll give you extensive training, and a growing responsibility for a wide variety of projects.

We expect that:

- you're a team player.
- you're an analytic problem solver.
- you're creative and eager to learn.
- you have a keen interest in digital embedded systems and software methodology.
- you have a Master of Science or PhD degree in Electronics Engineering (Embedded Systems and Multimedia, or Electronics and Integrated Circuits), Computer Science/Engineering, Applied Mathematics, or similar.
- you're fluent in English.
- you have a working knowledge of Dutch, since the language at the office is Dutch.

It's a plus if:

- you have some programming experience. E.g., in a university project, a contribution to an open-source project, as a hobby, etc. Show us your project on github!

You'll soon come into contact with:

- FPGA and digital ASIC design and verification
- (embedded) software design
- modeling and verification of large digital systems
- C++, SystemC, VHDL, (System)Verilog, GNU/Linux and easics in-house tools

You will work at the easics offices located in Leuven - Belgium. Structured work from home is possible up to 2 days per week.

easics is an equal opportunity employer. We value and recognize your talent with an attractive remuneration package.