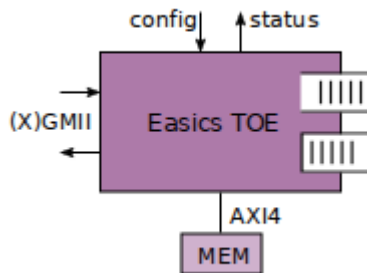


## TCP10G / TCP1G

The Easics TCP10G / TCP1G is an all hardware configurable IP core. It acts as a TCP server for sending and receiving of TCP/IP at maximal bandwidth and with very low latency. It does not require use of a processor.

The Easics TCP10G / TCP1G supports Ethernet packets, IP packets, ICMP packets for ping, TCP packets and ARP packets. The TCP10G additionally supports pause frames.



### Block diagram

### Features TCP10G & TCP1G

- Ethernet Jumbo Frame up to 9000 bytes supported
- Transmit and Receive buffers can be controlled to optimize the FPGA resource usage: 4kB up to 4GB per connection, internal SRAM or external memory.
- Guaranteed in-order reception of all data at the application side (FIFO interfaces)
- Fast response times to network traffic
- Integrated MAC layer
- Configurable MAC / IP address / TCP port
- ARP server for mapping IP address onto MAC addresses. No need to manually set the ARP table in the PC.
- ARP cache
- IPv4 unfragmented networking layer with a fixed (during connection) IP address (RFC791, RFC1042).
- ICMP echo protocol a.k.a. ping. This can be used for connectivity tests.
- 1 active server connection per TCP port
- Listens on fixed TCP port number, selectable at startup
- Configuration, status and statistics exported to pins on the core.
- 1G FIFO interface = 8bit @ 125 MHz
- 10G FIFO interface = 64bit @ 156.25 MHz
- TCP ACK piggybacking for reduced network load
- Packet retransmit, both fast retransmit and timeout retransmit, with exponential back-off
- Flow control, allowing backpressure from both server and client without data loss.
- TCP window size monitoring
- TCP Keep alive support (RFC1122)
- TCP Zero window probes
- TCP timestamps
- Nagle algorithm (Silly Window Syndrome)
- Round trip time measurement (RFC6298)

Core specifics	
Supported devices 1G	FPGA with 125 MHz capable IOs (most FPGA can do this, e.g. Xilinx Spartan6, Intel Cyclone V)
Supported devices 10G	FPGA with a transceiver that can do 10.3125 Gbit/s (Intel Arria 10, Intel Stratix, Xilinx Kintex 7 and up, Xilinx Virtex, ...)
Resource usage 1G	12K LUT
Resource usage 10G	36K Zynq LUT/ 22K Arria10 ALM
Provided with Core	
Design Files	Netlist for target FPGA
Example design	VHDL
Evaluation board 1G	Upon request
Constraints file	SDC
Simulation model	Precompiled Mentor Questasim library
Support	
Provided by Easics	

- Congestion Avoidance: slow start and congestion window
- Reordering for out-of-order packets
- PAWS (protection against wrapped sequence numbers)
- Very high throughput: > 99% of theoretical 10G bandwidth

### Features TCP10G

- Direct connection to a full duplex XGMII Ethernet PHY running at 10 Gbit with a fixed (during connection) MAC address. No MAC layer required.
- Pause frames

### Features TCP1G

- Direct connection to a full duplex GMII Ethernet PHY running at 1 Gbit with a fixed (during connection) MAC address. No MAC layer required.

## Overview

The TCP10G / TCP1G implements layer 2, 3 and 4 in the OSI reference model. Following standards/IETF RFCs are used in the implementation:

- Ethernet packets (IEEE 802.3–2012)
- IP packets (RFC791)
- ICMP packets for ping (RFC792)
- TCP packets (RFC793)
- ARP packets (RFC826)
- IP over Ethernet (RFC1042)
- TCP Keep alive (RFC1122)
- Congestion avoidance (RFC5681)
- Computing TCP's retransmission timer (RFC6298)
- TCP extensions for high performance (RFC7323)

## Clocking

Both 1G and 10G versions run on 1 clock. 125 MHz for 1G and 156.25 MHz for 10G.

## Interfaces

### 1G to physical layer

The core connects to a 1G PHY via a GMII interface. If the PHY has another interface (RGMII, SGMII), the protocol conversion can be done in FPGA logic.

### 10G to physical layer

The core connects to a 10G XGMII single data rate (SDR) interface. The XGMII interface is actually a double data rate (DDR) but that is not possible inside an FPGA. Therefore the interface is converted to SDR by doubling the databus.

Both Intel and Xilinx provide free IP cores for their transceivers that can connect directly to an SDR XGMII interface.

### 1G to session layer

A push side of a FIFO for the transmit side and a pop side of another FIFO for the receive side. Both are 8 bit wide and run @ 125 MHz.

If the rate at which data is removed from the FIFO is lower than the rate at which data arrives over the TCP link, the TCP window will fill up and the remote side will stop sending data. Once enough data is removed from the FIFO, the TCP core will notify the remote side to restart sending data (window inflation notification).

### 10G to session layer

A push side of a FIFO for the transmit side and a pop side of another FIFO for the receive side. Both are 64 bit wide and run @ 156.25 MHz. Since the TCP protocol is byte oriented, the fifo data contains an indication of how many bytes valid are each cycle (it can be less than 8 at the end of packet).

The behavior is the same as in the 1G version.

## Memory interface

Because memory requirements differ greatly per use case, the TCP buffer memory is not included in the core. Instead 2 AXI4 interfaces are provided that must be connected to the desired memory by the user.

Each AXI4 interface provides independent read and write interfaces. The write and read interface from the RX side must be connected to the same memory. The write and read interface from the TX side must be connected to the same memory. Connecting everything to the same memory instance is also allowed of course. The total memory bandwidth (read + write) should be more than 2 times the theoretical link speed for each direction (RX and TX). That is 2 Gbit/s for the 1G core and 20 Gbit/s for the 10G core. If RX and TX use the same memory, those numbers must be doubled.

## Configuration

The configuration interface for the core allows to set various parameters related to TCP, as well as basic Ethernet and IP parameters such as MAC and IP address. It can also be used to enable/disable various features inside the core (e.g. support for pause frames).

All the settings are pins on the core. They should only be changed when there is no TCP connection.

## Status

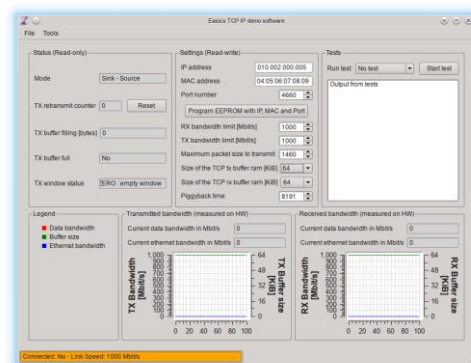
The complete TCP Protocol Control Buffer (PCB) as described in the RFC is exported to the user. It can be used to e.g. monitor TCP window sizes, memory usage, timers...

## Statistics

The statistics interfaces provide pulses for various events that occurs inside the core. The user can implement e.g. counters to keep track of the amount of packets, or the amount of retransmits that occurred.

## Demo

A development kit for TCP1G can be provided upon request. This development kit comes with the Easics TCP/IP evaluation software, containing a GUI to control all relevant parameters and measure the performance. For TCP10G a standard FPGA vendor board can be used.



Easics TCP/IP evaluation GUI