independent SoC design company

► ASIC
► FPGA
► embedded software

spin-off company of

► imec
► KU Leuven - ESAT
Located at the Arenberg Science Park in Leuven, Belgium
3 Pillars of Easics

RELIABILITY

CHALLENGE

FUTUR PROOF
About Easics

Easics is a **System-on-Chip design** company, targeting designs in digital & mixed-signal **ASICs** and **FPGAs**, and embedded software.

Easics designs **reliable** and **scalable high-performance & low-power** embedded systems for **leading product companies** active in wired & wireless connectivity, imaging / image sensors, multimedia, broadcast, industrial, medical / healthcare, (aero)space, and measurement equipment.

**Customers:**

- OEMs: electronics, optics, mechanics
- Semiconductor companies
- Analog / Mixed-signal IC design houses
Easics Organization

► **Board of directors & management**
  Chairman: professor André Oosterlinck
  CEO: Ramses Valvekens (representative of Boscant bvba)
  CTO: Steven Coenen (representative of Leonaster bvba)
  Founder: Jan Zegers
  Complemented by 1 administrative staff

► **Team: all MSc & PhD in Electronics Engineering / Computer Science**
  Architecture, Design, Verification, Integration, Lab Test: ASIC, FPGA, software
  Senior project leads
  Project leads
  Senior design engineers
  Design engineers

► **Team size: 17 people, growing each year**

► **Single location in Leuven, Belgium**
  500 m² of offices and lab space

► ** Entirely privately owned**
  Paid-up share capital is 1.561.500,00 EUR
Easics Customers Worldwide

► Europe

Belgium
The Netherlands
United Kingdom
Germany
France
Austria
Norway
Spain

► Rest of the world

USA
Japan
China
Australia
Israel
Mixed-signal ASICs
FPGA-based Embedded Systems
High-end Oscilloscopes & Spectrum Analyzers

Agilent Technologies

- Various ASIC developments
- Applications: generate and analyze next-generation wireless signals
- Low-power hand-held version
- Advanced Digital Signal Processing algorithms
- High performance
- High accuracy
- Compensation of analog imperfections
- Noise suppression of digital to analog
Cochlear hearing implant ASIC

- external device = microphones + DSP ASIC + battery + coil
- implanted = coil + ASIC + electrode array
- RF link
- high reliability
- ultra low-power
- incl. FPGA test environment development
Controller for in the Field Control of a High-Speed Measurement System using FPGA

- Xilinx Zynq FPGA with dual-core ARM Cortex A9 @ 667 MHz
- Runs GNU/Linux 3.19 with MMU support
- GNU C for ARM
- Dual DDR3 DRAM controller @ 800 MHz DDR (1600 Million transactions per second each)
- DMA controller for 10 Gbit/s packet rate
- Login over ssh, via Easics' 10Gbit/s Hardware TCP/IP core, over an 80 km optical fiber link (10GBASE-ZR+)
- Linux device drivers for custom peripherals:
  - Easics' 10Gbit/s Hardware TCP/IP core
  - TCP router
  - Transceivers
  - Clock monitoring
- Incl. embedded web-server

- Application: 
  - remote sensing
  - high throughput
  - low power: powered by solar cells
FPGA-based Optical Sorting Machine

- Real-time Image Processing for Optical Food/Non-Food Sorter
- Pipelined object delineation
- Object tracking
- Object properties & classification
- Position prediction
- Multi-camera
- Combined hardware processing & real-time software

See the machine in action:
http://www.youtube.com/watch?v=T3gPgLbIbnk
Companion ASIC for high-end scientific image sensors

- Radiation hardened ASIC
- Cryogenic temperature operation
- Fully programmable sequencer
- 16-bit A/D-convertors
- SpaceWire / RMAP interface
- Application: space science & earth observation missions
- Incl. FPGA test board development

DARE User Day @ ESA/ESTEC, 8 December 2014, Noordwijk, the Netherlands
https://indico.esa.int/indico/event/72/session/0/contribution/1/material/slides/0.pdf

Cryogenic and radiation hard ASIC design for large format NIR/SWIR detector array @ SPIE, 22-25 September 2014:
http://spie.org/Publications/Proceedings/Paper/10.1117/12.2067184

Bits&Chips Hardware Conference, 12 June 2013, ‘s-Hertogenbosch, the Netherlands:
http://bc-smartsystems.nl/_Resources/Persistent/0dec773c77410423a862b92c1eb1dfac364d544d/Geert%20Verbruggen.pdf

DSP Valley Newsletter, December 2012 / January 2013:

EE Times, 16 November 2012:
Companion ASIC for high-end scientific image sensors
Companion ASIC for high-end scientific image sensors

Cryogenic measurement setup: ASIC in liquid nitrogen + FPGA board
Image sensor ASIC for Leica M Camera

- Digital noise reduction
- Integrated on sensor chip

Easics successfully demonstrates Datapath Modeling Approach in CMOSIS Camera-Chip for the New “Leica M” Camera

Easics created a high-level model of the proprietary digital noise cancellation and correlated double-sampling algorithms for the CMOSIS “Leica M 24MP CMOS Sensor” chip. This model gradually proceeds over the textual specification document, while iteratively refining it. It becomes a bit true executable specification. Important executable use cases (main operational modes as well as corner case behavior) emerged naturally from this iterative refinement. They form the basis of the regression-based verification suite, and enable test-driven development. Easics used the model as reference for all verification. CMOSIS signed off on it, turning it into a formal decoupling point between the specification document and the detailed implementation.

Frequent specification changes are part of the game in leading-edge mixed-signal ASIC developments. In this development, they merely lead to iterations on the high-level model, rather than on detailed implementations (which would potentially cause major rework and schedule slips). The model-based approach is hence a key design productivity enabler, as the model is designed at the “right” level of abstraction for its purpose: right before converting the “what” into the “how”. It drastically improves the time-to-market and keeps the budget under control.

Easics further used the model as reference for the detailed implementation.

Read the full article:
Real-time image enhancement FPGA for thermal camera

On-the-fly high frame-rate non-uniformity compensation and calibration (non-uniformity changes with e.g., temperature)

Minimization problem, implemented on FPGA
Easics Core Business

- inside main circle: Easics Core Business
- outside main circle: performed by customer, supplier or subcontractor (long-term → partner)

SoC design services:
- digital ASIC
- FPGA

architecture

- analog ASIC
- ASIC supply
- IP licensing
- PCB supply
- PCB design
- software
- algorithms
Easics Collaborations

Long-term relationship with customers and partners
Easics Business Models

● Project-based design services: FPGA, ASIC, embedded software
  ■ Fixed-price with milestones
  ■ Time & materials

● IP licensing of Hardware IP cores

● R&D as partner or subcontractor in consortia
  ■ ESA, VLAIO (IWT) / ICON, Horizon 2020 / FP7, Catrene, Eurostars, CrossRoads, ...

● Sub-contractor / partner management & selection
  ■ Analog ASIC design & layout
  ■ ASIC supply: production, packaging, test → supply chain management
  ■ FPGA & ASIC IP cores
  ■ PCB design & layout
  ■ PCB supply: production, assembly, test

● Prototype Product delivery
  ■ Assembled & tested PCBs for FPGA-based embedded systems
  ■ Packaged & tested ASICs
Easics Customer Benefits

- Quality goal: 1st time right
- Short time-to-market ← Controlled schedule, short lab debug
- Designer productivity
- Uniformity ← Procedures + Tools
- IP:
  - Vast library of Easics Background IP → free to use by customer
  - Easics IP cores → shorter time-to-market

- No vendor lock-in
- Long-term reproducibility
- Reuse, scalability ← technology independent, software-approach
- Flexible partner, tracking project staffing needs → cost-efficient
- Long-term partner
- Consolidated Experience from many markets, customers, applications, domains, technologies, tools
  - ASIC Experience (and Methodology !) → advanced FPGA design
  - Wireline Communication (PDH, SONET / SDH, ATM, IP, …) Experience
    → reliable connectivity design
  - High Reliability Experience → design for space and rad-hard
Easics Quality DNA

2/2

- Easics maintains a Quality System for ASIC & FPGA design services
  - Continuous improvement
  - Procedures + [Tools & IP]
  - Regularly audited by Easics’ customers

- Design Services model (as opposed to Product delivery)
  ⇒ Easics can adapt to customer procedures
    - Upon customer request and mutually agreed upon at project start

- ⇒ Easics can interact directly with customer systems
  - e.g., revision control, issue tracking, quality reviews

- Customers in various markets & applications
  ⇒ Easics’ customers adhere to several standards:
    - ISO 9001:2008
    - NXP CoReUse
    - Space: ESA – ECSS, incl. ECSS-Q-ST-60-02
    - Medical: ISO 13485
    - Functional Safety: IEC 61508 → SIL-2, SIL-3

- Secured Back-up, secured shared repository with customer
Easics Training

- Personnel Selection: Job interview + technical tests
- On-the-job training
- Procedures + [Tools & IP]
- “Easics Academy”
  - Technical seminars organized at least once every month
- External training:
  - Technical courses: VHDL, ASIC / FPGA design flow, Functional Safety, …
  - Soft skill courses: writing documentation, project management, …
  - Technical Seminars by vendors: Intel [Altera], Xilinx, Microsemi [Actel], TSMC, ARM, Synopsys, Mentor Graphics, Cadence, MathWorks, …
  - Industry Workshops: ESA IP Cores Day, DSP Valley, cEDM PCB, Wireless Community, …
  - Industry Conferences: Embedded World (DE), Bits&Chips (NL), Image Sensors (UK), …
  - Academic Conferences: ESSCIRC, FPL (Field Programmable Logic)
- Easics teaching / lecturing for external audiences:
  - At universities, for master EE students: KU Leuven - ESAT, University of Ghent, …
  - At industry and academic conferences: Bits&Chips Smart Systems, SSIS, SPIE, …
- Easics Technical Library → book purchase policy

- Easics is a learning company.
Easics Rigorous Design & Verification Methodology

- Reusable, Evolvable, Scalable, Future-proof
  Technology-independent, High level of abstraction
  → through software thinking

- Regression-based verification

- Continuous Integration

- Languages:
  - SystemC, TLM, PSL
  - VHDL, Verilog
  - SystemVerilog / UVM
  - C++, C
  - Python, Ruby, tcl
  - Matlab
  - Verilog-A, Verilog-AMS, SystemC-AMS
Easics Reusable Verification in all Project Phases

Reuse in all project phases:
- Simulation
- FPGA prototype
- ASIC or FPGA product

Reuse of:
- Test Cases
- SW Driver code

Concrete example is shown for ESA – Companion ASIC & FPGA.
Easics Tools: QA, EDA (ASIC, FPGA, PCB), Software

- **Industry Standard Tools (commercial + open-source):**
  - Revision Control: `git` + path to SVN, ClearCase, DesignSync, ClioSoft, Perforce
  - Project management & issue tracking: **Redmine**
  - ASIC / FPGA / PCB design:
    - **Synopsys (incl. [Synplicity]), Cadence, Mentor Graphics, Intel [Altera], Xilinx, Microsemi [Actel], Lattice, Altium**
    - Software development: **GNU tool chain**: gcc, gdb, binutils, …
    - Numerical computation tools: **Matlab + toolboxes**, Scilab, Octave
  - GUI development: **Qt, Wt**

- **Complemented with Easics Tools (no vendor lock-in!):**
  - Hardware/Software co-simulation using FLI of Questa & Modelsim: [VHDL & Verilog] + [SystemC / C++, C, Python, tcl, Ruby, …]
  - Parallel (using multiple simulator licenses) regression simulations using dashboard and database: **reggie**
  - Hardware/Software co-design (register map generation): **VCI Compiler**
  - Interconnect-generator: **ariadne**
  - DSP / digital filter – generator (starting from Matlab)
  - Makefile generators: **cma (C/C++)**, **vma/sma** (VHDL/Verilog sim + synth)
  - Netlist sanity checker: **checknetlist**
  - Power analysis
Avoiding “Dead Ends”
Easics Approach → Project-based Design Services

- **Communication**
  - with scientists, system, software, digital & analog hardware, PCB, QA, marketing

- **Rigorous documentation throughout the project**

- **Requirements Engineering**
  - sensitivity analysis of req's → challenges & risks only @ your added value
  - missing information → we will unveil the unwritten requirements
  - conflicting information → we will resolve this with you
  - standards not yet stable → we will discuss with you

- **Feasibility + Architecture**
  - Modeling & Real-time algorithm development / refinement / optimization
  - technology & IP trade-offs and selection: technical + economical
  - future-proof, scalable, technology-independent architecture
    → product roadmap: better return-on-investment
    → support future technology migration
    → ↔ obsoleteness of components & tools

- **Implementation & Verification**
  - Physical validation in our labs
Easics Technologies

- **ASIC:** foundry-independent: TSMC, GLOBALFOUNDRIES, UMC, SMIC, ST, NXP, TowerJazz, LFoundry, ON Semi, X-FAB, ams, NEC, …
  - broad range of nodes: 16nm, 28nm, 40nm, 65 / 55nm, 90nm, 0.13μm, 0.18μm, 0.25μm, 0.35μm
- **FPGA:** vendor-independent: Xilinx, Intel [Altera], Microsemi [Actel], Lattice, …
  - incl. latest devices: ▶ Xilinx: UltraScale, 7-series & Zynq
  - ▶ Intel [Altera]: 10-series & SoC

- High-Speed links: copper (twisted-pair, coax) & optical fiber
- Embedded operating systems: Linux, eCos, …
- Embedded software + drivers
- PC Software, incl. GUI and drivers
- PCB → Easics' FPGA-centric approach:
  - FPGA SoC + DRAM + SRAM + power regulation + connectivity
  - (rather than “heterogeneous System-on-PCB”)

- Radiation tolerance:
  - imec / ESA - DARE library (UMC 0.18μm, 65nm upcoming)
  - various fault-tolerant techniques: TMR, watchdog, Hamming, …
## Easics Embedded Processors

1/2

### Processors integrated and Subsystems designed and integrated by Easics, include:

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Processor</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM</td>
<td>Cortex M0</td>
<td>low-power 40nm ASIC</td>
</tr>
<tr>
<td>ARM</td>
<td>Cortex M0+</td>
<td>low-power 90nm ASIC</td>
</tr>
<tr>
<td>ARM</td>
<td>dual Cortex A9</td>
<td>Xilinx Zynq FPGA</td>
</tr>
<tr>
<td>ARM</td>
<td>dual Cortex A9</td>
<td>Intel [Altera] SoC FPGA</td>
</tr>
<tr>
<td>ARM</td>
<td>ARM7TDMI</td>
<td>0.35μm ASIC</td>
</tr>
<tr>
<td>IBM</td>
<td>dual PowerPC 405</td>
<td>Xilinx Virtex-II Pro &amp; Virtex-4 FPGA</td>
</tr>
<tr>
<td>Xilinx</td>
<td>MicroBlaze</td>
<td>various Xilinx FPGAs</td>
</tr>
<tr>
<td>Intel [Altera]</td>
<td>Nios, Nios II</td>
<td>various Intel [Altera] FPGAs</td>
</tr>
<tr>
<td>Cadence [Tensilica]</td>
<td></td>
<td>0.13μm ASIC + Xilinx FPGA prototype</td>
</tr>
<tr>
<td>Cadence [Tensilica]</td>
<td></td>
<td>recent ASIC technology; design ongoing</td>
</tr>
<tr>
<td>NXP</td>
<td>CoolFlux BSP</td>
<td>low-power 40nm ASIC</td>
</tr>
<tr>
<td>NXP</td>
<td>CoolFlux HSP</td>
<td>65nm ASIC</td>
</tr>
<tr>
<td>NXP</td>
<td>CoolFlux DSP</td>
<td>low-power 90nm ASIC</td>
</tr>
<tr>
<td>Synopsys [Target Compiler]</td>
<td>BASE core</td>
<td>low-power 90nm ASIC</td>
</tr>
<tr>
<td>Cortus</td>
<td></td>
<td>architecture only</td>
</tr>
</tbody>
</table>
Open-Source Processors integrated and Subsystems designed and integrated by Easics, include:

<table>
<thead>
<tr>
<th>Aeroflex [Gaisler]</th>
<th>Leon Sparc</th>
<th>Xilinx FPGA for ASIC prototype</th>
</tr>
</thead>
<tbody>
<tr>
<td>Texas Instruments</td>
<td>OpenMSP430</td>
<td>0.18μm ASIC</td>
</tr>
</tbody>
</table>

- **Custom designed processors by Easics, include:**
  - Easics S8 Processor (IP available for licensing):
    - tiny microcontroller core with debug port
    - customizable with e.g., multiplier, divider, tailored memory interface
    - incl. software development tools
    - purpose: integration in mixed-signal ASIC
    - application: real-time control and sequencing
      system initialization and configuration
      system status monitoring

- Custom-made Network Processor:
  - packet processing
  - many-processor environment
  - hand-crafted hardware design
  - C-compiler generated using Synopsys [Target Compiler] tool chain
Easics Expertise

- **First-of-a-kind product development**
  - State-of-the-Art and beyond

- **High-performance Digital Signal Processing (DSP):**
  - Filtering of real-time sensor data, incl. biomedical signals
  - Wireless baseband processing: smartphones, healthcare applications
  - Software-defined radio (SDR)
  - Accurate measurement equipment: oscilloscopes, spectrum analyzers
  - Control systems

- **Ultra-low power design:**
  - Smartphone, batteryless UHF RFID tag, wearables for healthcare, ...

- **SoC integration:**
  - Processor selection
  - Hardware / software interface
  - Memory architecture
  - Integrate custom hardware, (multiple) embedded processor(s) and subsystem
  - Embedded software
Techniques
- Channel compensation, phase correction, bit alignment, framing, (un)bundling, …
- 8b/10b encoding, Trellis, Viterbi, CRC, …

Reliable Multi-Gigabit/s FPGA-to-ASIC connection schemes
- Easics designs applications containing both FPGA and ASIC

Standardized Protocols
- [various]: TCP/IP, Ethernet
- [various]: PCIe
- Wireline: xDSL / ATM (since 1995): e.g., for Alcatel Bell
- Wireline: SONET/SDH, ATM / IP (since 1995)
- Imaging: CoaXPress (video transport over Coax cable)
- Consumer: USB (since 1995): 1st in the world to demonstrate functional Silicon (both Device & Hub) for Philips Semiconductor (now NXP)
- Industrial: EtherCAT (real-time control, based on Ethernet)
- Space: SpaceWire (for ESA – European Space Agency)
- …
● TCP/IP stack, fully in hardware = Easics IP core for licensing
  ■ Available in 2 versions:
  ■ 10 Gbit/s: 10GBASE-R (copper) & 10GBASE-ZR+ (fiber)
  ■ 1 Gbit/s
  ■ Industry-record:
  ■ highest throughput: near 100% link utilization, independent of packet size
  ■ lowest latency
  ■ Core does not require processor or software-control.
  ■ Other end uses standard TCP/IP software stack.

● Multi-Gbit/s twisted-pair communication for image sensor read-out
  ■ environment: EMC-unfriendly
  ■ distance: several meters
  ■ I/O: LVDS

● Backplane connection transceivers: 10 Gbit/s

● Custom-made Network Processor
  ■ traffic management, shaping, queueing, switching, routing
Easics Expertise in Wireless Connectivity

- Several wireless ASIC & FPGA implementations
- Several (de)modulation schemes: QAM-64, QPSK, ...
- Full digital part of both Rx and Tx datapaths:
  from analog front-end till data packets in and out,
  incl. Automatic Gain Control (AGC) and Viterbi

- Satellite communication: DVB-S FPGA
- EPCGlobal Gen2 compliant UHF RFID Tag ASIC for aerospace
  ■ batteryless → RF power harvesting & backscattering transmitter
  ■ incl. FPGA prototype and FPGA-based test set-up
- GPS/Glonass/Galileo Receiver ASIC
- Software Defined Radio ASIC for LTE, gsm, EDGE, ...
- Bluetooth Low Energy (BLE) ASIC
- BLE Long Range ASIC
- DECT ASIC
Easics Expertise in Imaging Systems

Easics' vision/imaging customers include:

- image sensor manufacturers
- camera manufacturers
- system manufacturers

- video/image processing
- vision
- video/image interpretation
- DEEP LEARNING
- convolutional neural nets
- computational imaging

illumination

photons

lens

sensor

transmission

processing

Easics
Easics Expertise in Embedded Vision

- Combination of hardware (custom ASIC or FPGA) and embedded software (single processor or multi-core)
  - Hardware for high bandwidth (pre-processing + high-level processing)
  - Software for high complexity

- Architecture, HW/SW partitioning, algorithm development / refinement and implementation/verification in ASIC and FPGA

- Some realized examples → real-time processing on video stream:
  - Efficient algorithm implementation and bandwidth optimization
  - Extensive pipelining for real-time mathematical operator implementations
  - Custom, low-latency video compression / decompression
  - Streaming video over low-latency TCP/IP link purely in hardware
  - Camera interfacing and control
  - Noise reduction, correlated double sampling
  - Dilate / erode, various kernel filters, CORDIC algorithm
  - Codecs: run-length encoding, motion compensation, DCT, …
  - Object recognition, classification
  - Clustering / delineation
  - Hough-transform: finding objects having a known shape
  - 3D vision / DSP for time-of-flight camera
Easics Expertise in High Reliability

- **Fault Tolerance - Radiation Hardening – Functional Safety**
- **Space:** frame grabber FPGA for experiments at ISS, camera companion ASIC for NIR/SWIR detector, imager ASIC for meteorological satellite, ...
- **Medical:** - X-ray imaging equipment ASIC + FPGA
  - human body implant ASIC
- **Aerospace:** RFID tag ASIC
- **Defense:** full-custom camera FPGA
- **Industrial:** safety critical FPGA control system for process industry
Easics Datapath Modeling Approach
1/4

- **Start: problem definition**
  - not always possible to document in detail upfront

- **Model-based design**
  - avoid (expensive) design iterations in hardware
  - high-level model = **software algorithm** running on a PC → exploration
  - software language = customer preference:
    - C++/SystemC, Matlab, Python, Ruby, … (<> VHDL, SystemVerilog, …)
  - use of existing 3rd party software libraries
  - “no restrictions”
  - data model: configuration parameters + status

- **Software algorithm = investment → reuse**
  - early demonstration
  - hardware implementation:
    - regression-based verification
    - same data model
  - product roadmap: scalability → future products
● **→ Specification (“WHAT”):**

Through iterative refinements (with the customer), the model gradually becomes a bit-true executable specification.

● This includes verification:
  
  **use cases** emerge naturally:
  - main modes
  - corner cases

● “visual” checks (for image / video processing)

● **⇒ Hand-off to:**
  - Software team @ customer for early demonstrations
  - Hardware architecture & implementation
Easics Datapath Modeling Approach
3/4

- **→ Hardware architecture ("HOW"):**

- Based on “WHAT” + **constraints**: performance, area (cost), power consumption, algorithm maturity, project schedule, ...

- Profiling (hotspots, bottlenecks)

- **Hardware architecture:**
  - Hardware/Software interface
  - Memory organization
  - Parallelization, pipelining, resource sharing
  - Mathematical operator implementation
e.g., CORDIC algorithm
  - Power strategy: clock gating, power gating, ...
- **Hardware implementation:** VHDL RTL → ASIC or FPGA
  - experience-based
  - build on known concepts
  - limited iterations
  - complemented with:
    - code-generators
    - high-level synthesis (HLS)
    - verification: simulate against model (= spec) + use cases

- **Future reuse for follow-on products:**
  - more efficient to start from a software model than to start from an optimized hardware implementation of a few years ago …

Read more about Easics Datapath Modeling Approach in the DSP Valley Newsletter, December 2012 / January 2013:

Intellectual Property available for licensing: Hardware IP Cores for FPGA & ASIC

- **TCP/IP stack:**
  
  2 versions available:
  - 10 Gbit/s
  - 1 Gbit/s

- **DDRx memory controllers**

- **S8:** Tiny customizable microcontroller core
  - with debug port
  - incl. software development tools
  - for integration in mixed-signal ASIC

- **CoaXPress interface**

- **SATA interface towards Solid State Drive (SSD): to be announced**
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