

EASICS NV – Company Presentation

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www.easics.com

About EASICS NV

Unified Design Flow

Digital Design Styles

ASIC Prototyping

Application 1 : Multi-standard Telecom chip

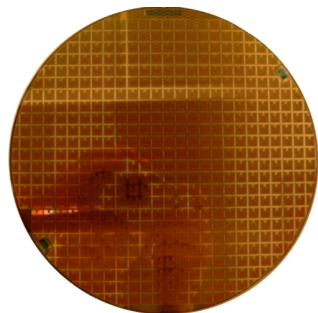
Application 2 : Parallel Digital Image Processing

Application 3 : Radio Frequency Identification (RFID)

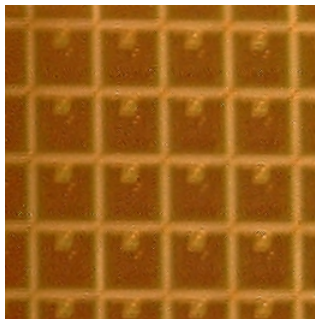
Coordinates

About EASICS NV

Core Business



- ▶ EASICS NV is founded in 1991
- ▶ Spin-off from IMEC & K.U.Leuven
- ▶ Independent Design & IP Company
- ▶ EASICS designs **Digital Systems**, including **Embedded Software** :
 - ▶ Digital ASIC
 - ▶ Mixed-signal ASIC
 - ▶ Structured ASIC
 - ▶ FPGA
 - ▶ FPGA Prototype for ASIC
 - ▶ System-on-Chip
- ▶ Focus on the Application (↔ Technology)



- ▶ EASICS' **Added Value** :
 - ▶ Independent Study
 - ▶ Requirements Tuning
 - ▶ Design Methodology & Tools
 - ▶ Expertise & IP in Connectivity, Multi-Processor & DSP
 - ▶ Architecture Design
 - ▶ Technology-independent Implementation ⇒ Future-Proof
- ▶ EASICS works with **Partners** :
 - ▶ PCB design, production & test
 - ▶ Analog design
 - ▶ Chip layout
 - ▶ Chip production, packaging & test

About EASICS NV

- ▶ EASICS is active in the following markets :
 - ▶ Industrial Automation & Machine construction
 - ▶ Wired Telecom
 - ▶ Wireless Telecom
 - ▶ Consumer Electronics
- ▶ Some recent designs :
 - ▶ **Machine-control** based on image processing on multi-processor architecture : FPGA
 - ▶ **RFID Tag** (Radio-Frequency Identification) : FPGA Prototype + Mixed-signal ASIC + Software
 - ▶ **Telecom chips** for optical-fiber communication (SDH/SONET), Ethernet, xDSL, ...
 - ▶ **High-Accuracy Measurement Equipment** : Mixed-signal ASIC incl. DSP
- ▶ Customers :
 - ▶ Belgium : 1/3
 - ▶ Europe (excl. Belgium) : 1/3
 - ▶ USA : 1/3

About EASICS NV

This is why customers worldwide select EASICS for their next chip and FPGA developments :

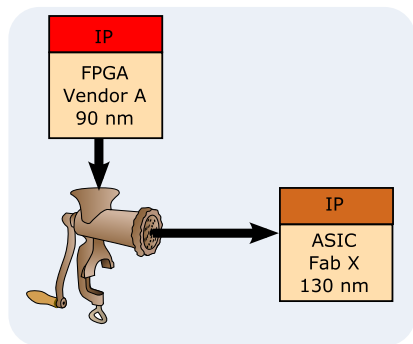
- ▶ We select technologies that fit our customers' business case.
- ▶ We finetune the chip's requirements, to prolong its "expiry date", in spite of new and "in flux" standards.
- ▶ We have a unique verification strategy based on EASICS' tools that drastically shortens the time-to-market.
- ▶ We use our unparalleled expertise in packet processing now in new application domains of connectivity including wireless.
- ▶ We have demonstrated skills in integrating critical digital and analog functions on the same chip.
- ▶ We design ASICs in many technologies and process generations including the most recent 65 nanometer.
- ▶ We are equally competent in FPGA design, using techniques from the ASIC world, resulting in substantially higher quality-of-results.

EASICS' Unified Design Flow

- ▶ Technology-independent
 - ▶ vendors, technology generations
 - ▶ ASIC + FPGA (prototype/emulation or final product)
- ▶ Hardware + Software
- ▶ Digital + Analog (Mixed-signal) : Test, bypass, STA, ...
- ▶ Reuse of Verification at all levels
 - ▶ computer simulations at RTL & gate-level
 - ▶ measurements on FPGA prototype and/or emulation
 - ▶ measurements on ASIC
 - ▶ measurements on ASIC at customer of ASIC supplier
- ▶ Combination of CAD Tools
 - ▶ Commercial EDA Tools : Mentor Graphics, Synopsys, Cadence, Synplicity, Denali
 - ▶ EASICS Tools
 - ▶ Open-Source Tools : GNU/Linux, gcc, git

Digital Design Styles

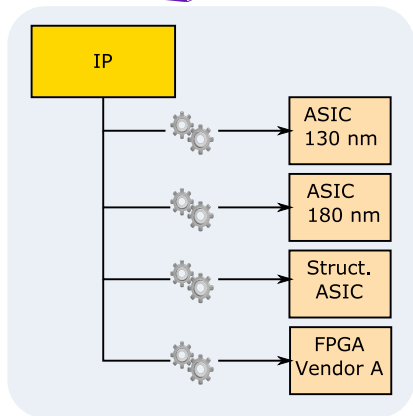
Started Technology-specific ...



- ▶ FPGA(s) → (Struct.) ASIC when volumes get larger
- ▶ ASIC → other ASIC because 1st supplier stops that technology
- ▶ ASIC → other ASIC as second source, or to newer technology
- ▶ Mature ASIC → FPGA (we have 65 nm FPGAs now!)
- ▶ Reuse in a new chip : but now faster and more channels
- ▶ ...

Digital Design Styles

EASICS' Technology-independent Design \Rightarrow Future-Proof



- ▶ Requirements
- ▶ Methodology
- ▶ Design Partitioning
- ▶ Coding style (C++, C, Matlab, VHDL, Verilog, ...)
- ▶ IP blocks ?
- ▶ Synchronous design
- ▶ Clocking strategy
- ▶ Testability
- ▶ Verification
- ▶ ...

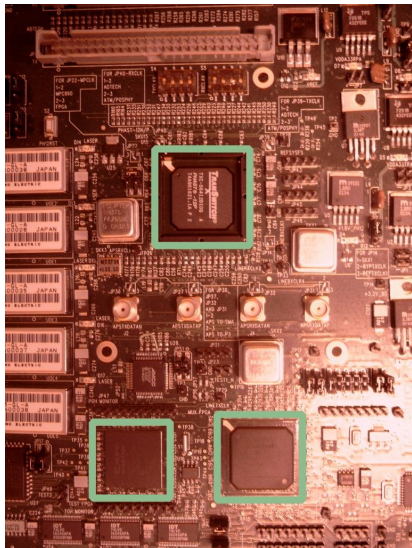
ASIC Prototyping

- ▶ **Generic prototyping main board**
large FPGA(s) + connectors + voltage regulation
- ▶ **Generic plug-in daughter boards**
e.g., SRAM, SDRAM, DDRx, Ethernet, USB, ...
- ▶ **Application-specific plug-in daughter boards**
e.g., A/D, D/A, optical link, ...

Combined with technology-independent design techniques, this approach allows for fast prototyping (no large PCB needs to be developed), at ASIC speed (using 90nm or 65nm FPGAs), and early firmware development, while the ASIC and its detailed requirements are still in development.

Multi-standard Telecom chip

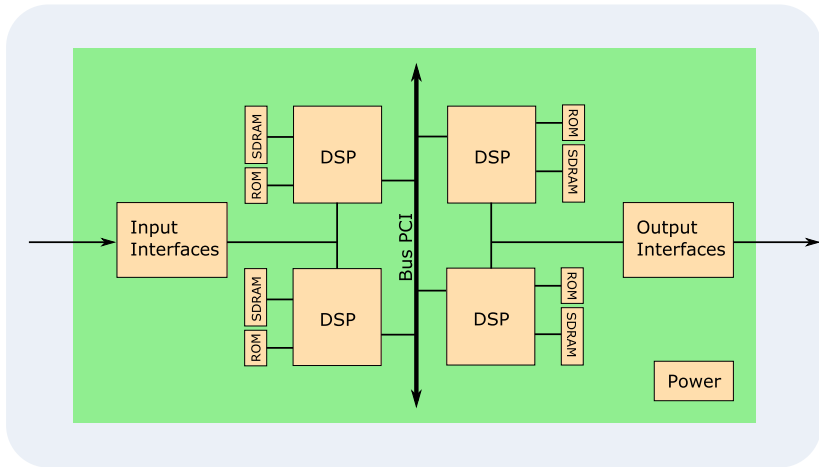
Technology-independent Design



- ▶ Design of reusable & scalable IP library
- ▶ Implementation of 180 nm ASIC (top)
- ▶ Interoperability with future 130 nm ASIC demonstrated using FPGAs (bottom)

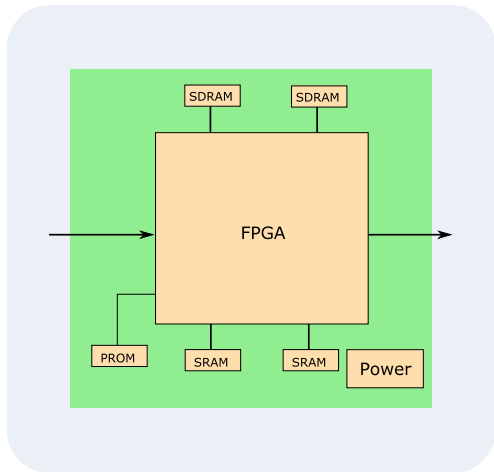
Parallel Digital Image Processing

Classical Architecture : Four DSP Processors



Parallel Digital Image Processing

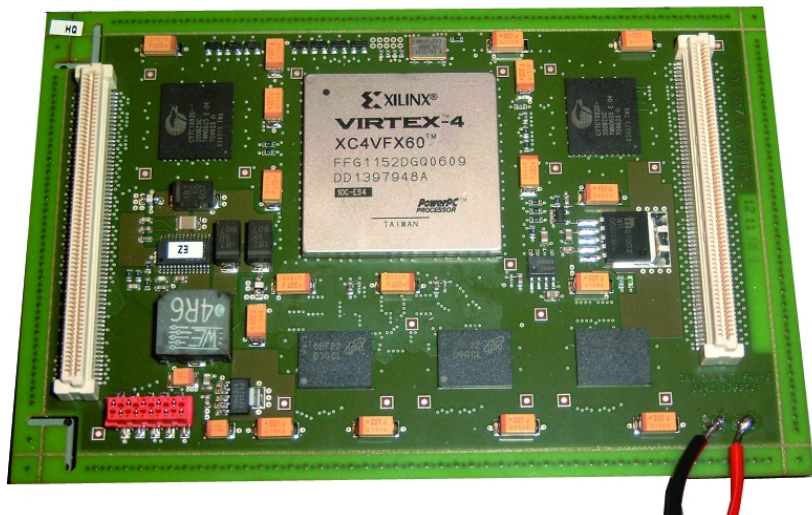
Flexible Architecture : Single FPGA using Array of Softcores & Hardware DSP



- ▶ Central FPGA using Array of Softcores
- ▶ Future applications can be supported **on the same PCB** :
 - ▶ modify Software
 - ▶ add Softcores
 - ▶ add other Logic
 - ▶ use larger size FPGA (footprint compatible)

Parallel Digital Image Processing

Flexible Architecture



Radio Frequency Identification (RFID)



- ▶ Aerospace industry
- ▶ Pharmaceutical industry
- ▶ Retail distribution
- ▶ ...



Handheld Reader ↔ Fixed Reader @ Gate

Radio Frequency Identification (RFID)

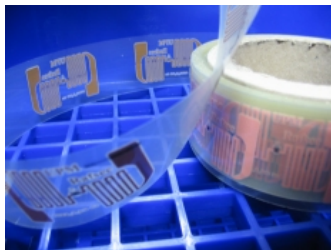


Applications :

- ▶ Supply Chain Management
- ▶ Asset Tracking
- ▶ Authentication

Combination of skills :

- ▶ Antenna on foil
- ▶ Analog : RF, NVM, ESD
- ▶ Digital : connectivity, processing
- ▶ Mixed-signal integration
- ▶ Ultra-low power



EASICS designs next-generation Tags.



- ▶ EASICS NV is based in Leuven, Belgium
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